Notice of Allowability	Application No.	Applicant(s)	
	10/785,557	ROOHPARVAR ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *27 September 2004*.

2. ☒ The allowed claim(s) is/are *1-4,8-12,14-17 and 19-21*.

3. ☒ The drawings filed on *24 February 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

1. Applicant's Terminal Disclaimer filed September 27, 2004 has been approved.

Election/Restrictions

2. Due to the non-serious burden upon the examiner for searching the species set forth in the Election Requirement mailed in June 22, 2004, the Election Requirement is hereby withdrawn. As a result, applicant's cancellation of claims 16 – 21, as filed in the Response to the Election/Restriction Requirement in July 21, 2004, has been withdrawn. Confirmation of such withdrawal was given in a telephone interview with applicant's attorney, Mr. Kenneth W. Bolvin (reg. no. 34,125) in November 5, 2004.

All initially submitted claims as filed in February 24, 2004, and later renumbered according to rule 1.126 in June 07, 2004 as also indicated in the Election Requirement, are now pending.

3. Claims 1 – 21 are presented for the present examination.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in the telephone interview with Mr. Kenneth W. Bolvin (reg. no. 34, 125) on November 5, 2004.

The application has been amended as follows:

Replace all previously presented pending claims with the following revised and amended claim set.

1. A flash memory device comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal comprising clock cycles;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections;

sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell; and

command logic coupled to the array to provide two data access operations per clock cycle, wherein the command logic includes control registers used to store data for memory operation control.

2. The flash memory device of claim 1, wherein the array of non-volatile memory cells is arranged in a plurality of addressable banks.

3. The flash memory device of claim 2, wherein each addressable bank contains addressable sectors of memory cells.

4. The flash memory device of claim 1, wherein the data connections are burst oriented and the command logic comprises means for starting data access at a selected location and continuing for a programmed number of locations in a programmed sequence.

5. The flash memory of claim 1, wherein the pre-charge circuitry pre-charges an active digit line that is coupled to a read memory cell to a voltage that is greater than a complementary digit line.

6. The flash memory of claim 1, wherein the pre-charge circuitry pre-charges the bit lines to a differential level using charge sharing.

7. The flash memory of claim 1, wherein the pre-charge circuitry pre-charges the bit lines to a differential level using a bias circuit.

8. A processing system comprising:

a processor; and

a rambus dynamic random access memory compatible flash memory device coupled to the processor, the memory device comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal comprising clock cycles;

a rambus dynamic random access memory interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented;

sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell; and

command logic coupled to the array to provide two data access operations per clock cycle starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

9. The system of claim 8, wherein the processor generates flash memory compatible control signals.

10. The system of claim 8, wherein the processor is adapted to receive burst transmissions of data from the memory device.

11. The system of claim 8, wherein the non-volatile memory device is a flash memory device.

12. A processing system comprising:

a processor;

a single communication bus coupled to the processor;

a volatile memory device coupled to the single communication bus; and

a rambus dynamic random access memory (RDRAM) compatible flash memory device coupled to the single communication bus, the memory device comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal comprising clock cycles;

sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell; and

command logic coupled to the array of non-volatile memory cells to provide two data access operations per clock cycle following an RDRAM compatible format and starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

13. The processing system of claim 12, wherein the volatile memory device and the RDRAM compatible flash memory device both respond to common command signals provided on the single communication bus.

14. The processing system of claim 12, wherein the two data access operations per clock cycle are performed on clock transistions.

15. The processing system of claim 12, wherein the memory cells are floating gate memory cells.

16. The processing system of claim 12, wherein the processor generates computer system commands.

ii. Original claims 5 – 7, 13, and 18 are cancelled.

5. The following is an examiner's statement of reasons for allowance:

The prior arts teach a flash memory device comprising:

an array of non-volatile memory cells; a clock signal connection to receive a clock signal comprising clock cycles; data connections; and sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines.

However, the prior arts did not teach the flash memory device, further comprising:

an RDRAM interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus; command logic coupled to the array to provide two data access operations per clock cycle wherein the command logic includes control registers used to store data for memory operation control; and pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham
October 26, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800